

# DW03MFC-B-S

Order Code: DW03MFC-B-S

#### **Transient Voltage Suppressor**

#### **Features**

- Solid-state silicon-avalanche technology
- 200 Watts Peak Pulse Power per Line (t<sub>p</sub>=8/20μs)
- Low operating and clamping voltages
- Protects five I/O lines
- Working Voltages: 3.3 V
- Low Leakage Current

### IEC COMPATIBILITY (EN61000-4)

- IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 15A (8/20μs)

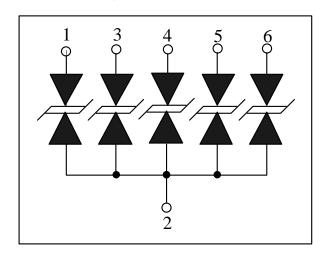
#### **Mechanical Characteristics**

- SOT-563 package
- Molding compound flammability rating:
  UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS Compliant

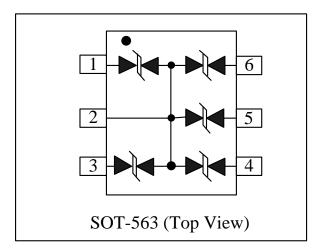
#### **Applications**

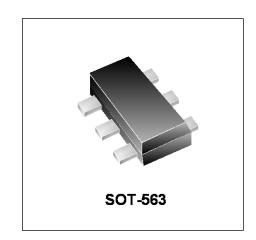
- Cellular Handsets & Accessories
- Personal Digital Assistants (PDAs)
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- MP3 Player

### **Circuit Diagram**



## **Schematic & PIN Configuration**

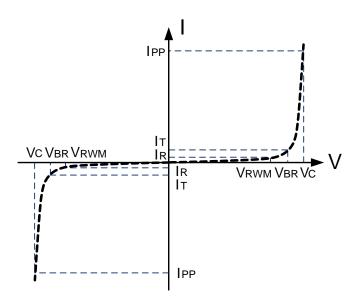




Absolute Maximum Rating							
Rating	Symbol	Value	Units				
Peak Pulse Power ( t <sub>p</sub> =8/20μs )	P <sub>PP</sub>	200	Watts				
Peak Pulse Current ( t <sub>p</sub> =8/20µs )	Ірр	15	А				
Operating Temperature	TJ	-55 to + 125	°C				
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C				

# Electrical Parameters (T=25°C)

Symbol	Parameter	
<b>I</b> PP	Reverse Peak Pulse Current	
Vc	Clamping Voltage @ IPP	
V <sub>RWM</sub>	Working Peak Reverse Voltage	
IR	Reverse Leakage Current @ V <sub>RWM</sub>	
V <sub>BR</sub>	Breakdown Voltage @ Ιτ	
lτ	Test Current	
l <sub>F</sub>	Forward Current	
VF	Forward Voltage @ I <sub>F</sub>	



### **Electrical Characteristics**

DW03MFC-B-S							
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	
Reverse Stand-Off Voltage	V <sub>RWM</sub>				3.3	V	
Reverse Breakdown Voltage	$V_{BR}$	I <sub>T</sub> =1mA	3.7			V	
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> =3.3V,T=25°C			100	nA	
Peak Pulse Current	Ірр	t₂=8/20µs			15	А	
Clamping Voltage	Vc	I <sub>PP</sub> =15A, t <sub>p</sub> =8/20µs			12	V	
Dynamic Resistance <sup>1,2</sup>	R <sub>DYN</sub>	Tlp=0.2/100ns		0.202		Ω	
Junction Capacitance	C <sub>j</sub>	Between I/O pins and Ground V <sub>R</sub> = 0V, f = 1MHz		15	18	pF	

#### Notes

- 1、TLP Setting:  $t_p$ =100ns,  $t_r$ =0.2ns,  $I_{TLP}$  and  $V_{TLP}$  sample window: $t_1$ =70ns to  $t_2$ =90ns. 2、Dynamic resistance calculated from  $I_{PP}$ =4A to  $I_{PP}$ =16A using "Best Fit".

### **Typical Characteristics**

Figure 1: Peak Pulse Power vs. Pulse Time

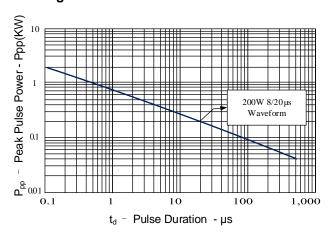


Figure 2: Power Derating Curve

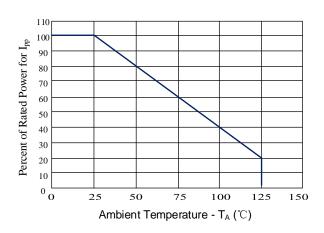


Figure 3: Clamping Voltage vs.Peak Pulse Current

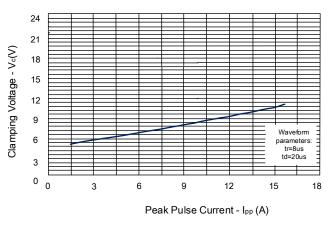


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage

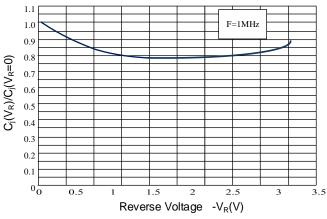


Figure 5: TLP Positive I-V Curve

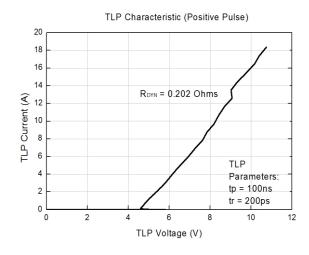
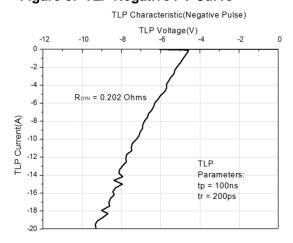


Figure 6: TLP Negative I-V Curve



#### **Application Information**

The DW03MFC-B-S was designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides bidirectional protection; the device is connected as follows:

#### **BIDIRECTIONAL COMMON-MODE CONFIGURATION**

The DW03MFC-B-S provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 6. Circuit connectivity is as follows:

- I/O 1 is connected to Pin 3.
- I/O 2 is connected to Pin 1.
- I/O 3 is connected to Pin 6.
- I/O 4 is connected to Pin 4.
- Pin 2 is connected to ground.

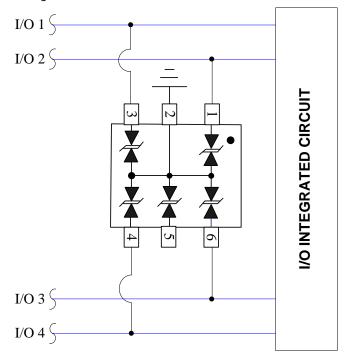


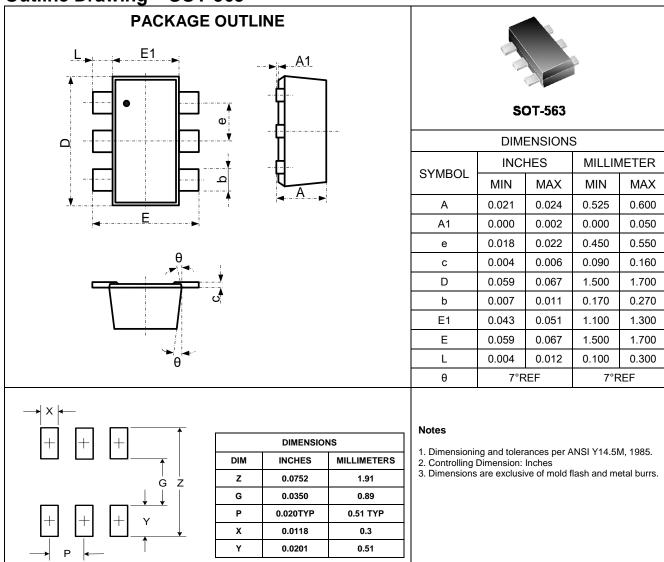
Figure 6 Bidirectional Configuration Common-Mode I/O Port Protections

#### **CIRCUIT BOARD LAYOUT RECOMMENDATIONS**

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

# **Outline Drawing - SOT-563**



## **Marking Codes**

Part Number	DW03MFC-B-S
Marking Code	B3FC

## **Package Information**

Qty: 3k/Reel